Robust Method of Fabricating Epitaxially Encapsulated MEMS Devices with Large Gaps

Yunhan Chen, Ian B. Flader, Dongsuk D. Shin, Chae Hyuck Ahn, Janna Rodriguez, and Thomas W. Kenny

***Abstract*— This paper presents a novel wafer-level thin-film encapsulation process that allows both narrow and wide trenches, which are necessary for traditional structures such as comb-drives. Fully functional devices with trench widths up to 50 μm are fabricated by employing a vapor phase XeF_2 isotropic silicon etch to create large cavities and an epitaxial deposition seal to encapsulate the devices in an ultra-clean, high vacuum environment with no native oxide and humidity. In this paper, we demonstrate the robustness of the proposed fabrication process, as well as the inherent benefits of the high-temperature epitaxial encapsulation process: high quality factor, extreme stability, exceptional aging, and fatigue performance. [2017-0098]**

***Index Terms*— Wafer-level encapsulation, epi-seal, hermetic packaging, micromachining, XeF_2 isotropic etching, wide gap.**

I. Introduction

PACKAGING of micro-electromechanical system (MEMS) is critical for protecting the devices from external variations, as well as for providing a stable operating environment [1]. It is especially essential in high performance applications, as any contamination or excessive pressure may degrade the device performance severely [2]. Traditional chip-level packaging techniques, which involve assembling of individual device chips with packaging after singulation, often suffer from high cost and low yield. On the other hand, wafer-level packaging has shown the potential to improve yield and device performance with low cost. Anodic or eutectic wafer bonding [3], [4] and thin-film encapsulation [5], [6], the two most common wafer-level packaging methods, have been demonstrated in both research and commercial settings.

The *epi-seal* encapsulation process is a wafer-level thin-film encapsulation method that was proposed by researchers at the Robert Bosch Research and Technology Center in Palo Alto and demonstrated in a close collaboration with Stanford University. Exceptional cleanliness, stability, robustness [7] and its fatigue-free material property [8] make the *epi-seal* process an ideal platform for fabrication and packaging of silicon MEMS resonators. The baseline *epi-seal* process has been successfully adapted in commercial products by SiTime Inc. [9], [10].

The standard *epi-seal* process utilizes sacrificial low pressure chemical vapor deposition (LPCVD) silicon dioxide to fill and bridge the lateral device trenches. Upon removal of the sacrificial oxide with vapor phase hydrofluoric acid (HF) after the deposition of the polysilicon encapsulation layer, released devices are re-sealed in ultra-clean, native oxide-free, and low-pressure cavities. LPCVD Tetraethylorthosilicate (TEOS) oxide used as the sacrificial material is conformal; however, it has a slow overall deposition rate ($\sim 0.4 \mu$m/hr) and an expensive tool overhead. In addition, a stress-relieving annealing step for every 1μm of oxide deposition is required to prevent the oxide film from cracking. As the oxide thickness accumulates, it becomes impractical to deposit a large amount of TEOS oxide to fill wide trenches. For this reason, the maximum device trench width is usually limited to 1.5μm with 2$\sim$3 cycles of deposition and annealing. This precludes the fabrication of structures such as comb-drives, as well as devices with large lateral displacement. To encapsulate larger trenches in the baseline *epi-seal* process, several solutions have been previously proposed.

In an effort to encapsulate devices with wider gaps in *epi-seal*, Ayanoor-Vitikkate *et al*. [11] proposed to use the oxidation of sacrificial silicon beams to fill the large trenches with silicon dioxide, which will subsequently be etched away with vapor phase HF (vHF) after encapsulation. Uniformly sized silicon beams are first patterned and etched in the large gap area, followed by a carefully timed thermal oxidation to fully convert all the silicon beams into silicon dioxide while reducing the gap size in between. Device gaps as wide as 20μm were encapsulated with this method. However, this process has several limitations. First, the width of trenches can only be a multiple of the sacrificial silicon beams' fixed width and interval gap. Second, any insufficient oxidation of the sacrificial silicon will result in entrapment of small silicon pieces inside the cavity, resulting in shorting of devices. Furthermore, the oxidation step also enlarges narrow gaps, making this process unsuitable for fabricating devices that require small and precise transduction gap widths. Large amounts of oxidation also cause various stress issues during the fabrication. No functional devices have yet to be demonstrated using this proposed method.

Previous work by Graham *et al.* [12] used plasma enhanced chemical vapor deposition (PECVD) oxide—which has a

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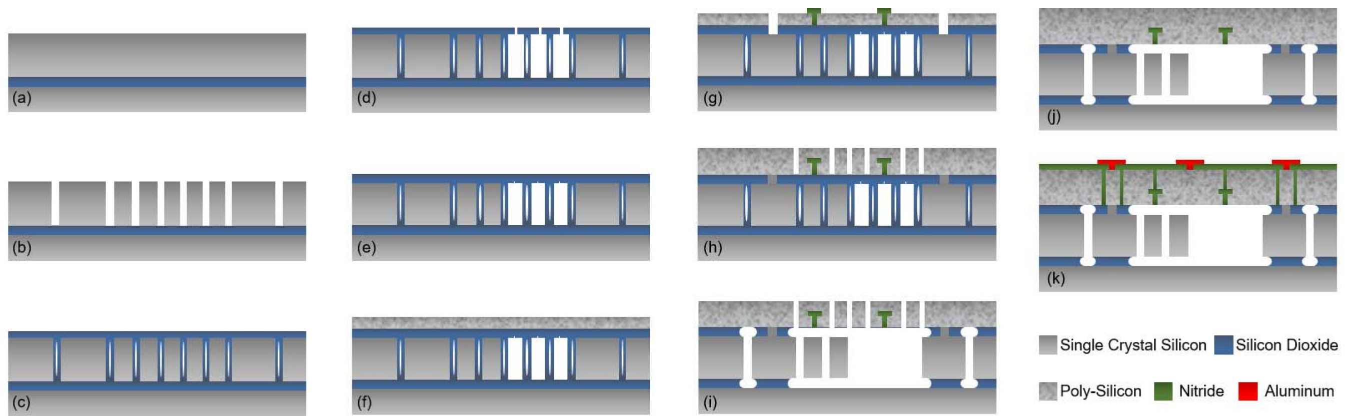

Fig. 1. Process flow of the encapsulation process, showing the cross-section schematic: (a) SOI wafer preparation; annealing and alignment marks patterning; (b) Device layer etching; (c) Sacrificial LPCVD oxide deposition; (d) Pinhole patterning and XeF_2 etching to form large cavities; (e) Pinhole sealing with more LPCVD oxide; (f) First epitaxial polysilicon layer deposition; (g) Creating nitride etch stops for top electrode isolation and electrical contact to device layer; (h) More epitaxial polysilicon deposition and vents patterning; (i) Releasing of sacrificial oxide with vapor HF; (j) Final sealing; (k) Creating electrical isolation and metallization for bond pads and metal traces.

much faster deposition rate (1μm/min)—to directly fill trenches up to 20μm. Partial planarization of a thick sacrificial oxide exceeding 20μm in thickness is essential. Due to the limitations of the planarization method, however, the final oxide spacer surface is non-uniform and its thickness varies widely between wafers. Pinch-off often forms above the silicon surface due to the non-conformal deposition of PECVD oxide. During planarization, these keyholes open up and cause the deposition of the silicon inside the cavity. Moreover, thick oxide films build up stress on the wafers, limiting the maximum amount of oxide deposition and requiring careful monitoring of the wafer bow. Despite the intrinsic irregularities introduced by this process, working devices have been demonstrated.

Instead of filling the wide trenches with sacrificial silicon dioxide, Massana *et al*. [13] combined fusion bonding and epitaxial sealing. Yang *et al*. [14] further modified this process to realize a unified *epi-seal* process that incorporates large gaps, etch hole-free structures and top electrodes at the same time. These relatively straightforward processes have demonstrated working devices that preserve the *epi-seal* process' key advantages, such as ultra-clean and low-pressure cavities. However, wafer bonding and grinding steps have proven to be highly problematic: any particles or uneven surfaces cause voids during wafer bonding, which reduces yield for large structures. Furthermore, these voids may form craters on the wafer surface if the voids explode in later steps. Even if no visible voids are observed, it has been reported that vapor HF can release unwanted areas through hidden pathways on the bonding interface, causing delamination of the encapsulation layer. Stress-induced wafer bow issues have also been observed.

This paper is based on the technique presented in [15] for fabricating large cavities. Here, we demonstrate a robust, wafer bonding-free fabrication process that allows hermetic encapsulation of devices with precise narrow and large trenches. While maintaining all the key features of *epi-seal* process, the proposed process only adds a few additional steps in which

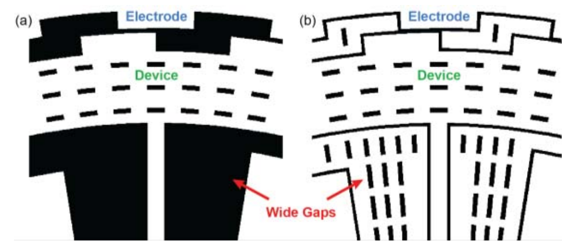

Fig. 2. Device layer design comparison between (a) traditional process and (b) the proposed process. Figure shows a section of a wheel shaped resonator. Patterns in black are defined trenches.

vapor phase XeF_2 isotropic etching of sacrificial silicon is used to create large gaps. Fully functional devices with lateral gaps as wide as 50μm are demonstrated while the integrity of the narrow gaps is preserved. The later sections of this paper are organized as follows: In §II, detailed process flow is presented. Device performance is discussed in §III, where measurements on frequency response, cavity pressure, stability and wafer stress are presented. Future process improvements are discussed in §IV. Finally, concluding remarks are presented in §V.

II. Process Flow

Silicon-on-insulator (SOI) wafers with 20μm device layers were used in the process of this work (Fig. 1(a)). All wafers have a 2μm-thick buried oxide (BOX) layer. Prior to processing, the wafers are annealed for 20 hours at 1100°C to relieve any residual stress from the SOI wafer fabrication.

A. Device Layer Trench Etching

As show in Fig. 1(b), Deep Reactive Ion Etching (DRIE) of the device layer is performed with a Surface Technology System (STS) Pegasus etch tool. As shown in Fig. 2(a), large trenches are directly patterned and etched in the traditional process. In this work, only narrow trenches ($<1.5\mu$m) are etched around the perimeter of the large gap area, as well as

small slots which, in later steps, will serve as support pillars to prevent the oxide diaphragm from buckling (Fig. 2(b)). Silicon in the large gap area will be removed in later steps to form large cavities.

As reported in [12], it is often difficult to optimize DRIE recipe for trenches with various sizes. To achieve precise trench widths and to reduce the lateral etching of trenches, increasing the passivation or decreasing the etch time and power for each cycle is desired. However, for large trenches, grassing will be observed due to the excessive amount of polymer if passivation is increased or etching time is decreased. Trade-off between the trench profile and grassing is unavoidable in the traditional process. In the process demonstrated in this work, the DRIE recipe can be optimized solely for narrow trenches, eliminating the risk of grassing. Thus, this work allows for more precise trench widths for all trench sizes, in comparison with previous works in which narrow and large trenches need to be etched with a single DRIE step. The DIRE recipe used in this work is summarized in [15].

B. Sacrificial Oxide Deposition

LPCVD TEOS oxide, which is used as a sacrificial material later in the vapor HF releasing step, is deposited to create the separation between the device layer and the cap. To prevent the polysilicon from depositing into trenches, the sacrificial oxide must completely bridge the lateral gaps with minimal surface topology. However, the large time consumption of filling wide lateral trenches with sacrificial oxide and the difficulties in planarization not only limit the trench width, but also prevent standard methods from being robust, high-yield processes. In this work, as only narrow trenches up to 1.5μm wide are etched, all trenches can be easily filled with conformal LPCVD TEOS oxide. As shown in Fig. 1(c), narrow trenches in the device layer are filled, and a 1.2μm oxide film is left on the top surface. As will be described in the following sections, the silicon under the oxide film will be removed by isotropic vapor phase XeF_2 etching to form wide cavities, leaving the thin oxide film bridging over the large trenches.

C. XeF_2 Etching to Create Large Cavities

Pinholes with 0.7μm diameter are etched through the 1.2μm oxide film atop the large trench areas with Applied Materials P5000 Etcher, exposing a pathway for vapor phase XeF_2 silicon etching. SPTS Xactix XeF_2 Release Etch System is used to remove the sacrificial silicon in the large trench areas through the pinholes (Fig. 1(d)). The choice of using XeF_2 etching is based on two considerations. Firstly, vapor phase XeF_2 is isotropic which allows the removal of sacrificial silicon through the small pinholes that can be subsequently sealed. Secondly, comparing with other possible silicon etching methods such as using RIE with SF_6 gas, the high selectivity (>1000:1) of the XeF_2 etching of silicon to oxide allows the complete removal of sacrificial silicon with the thin oxide film intact.

Fig. 3 shows the comparison of the structures without and with XeF_2 etching, as seen through an optical microscope. As shown, the LPCVD oxide that was filled into the narrow trenches serves as etch stops, preventing the surrounding silicon structures from being etched. Fig. 4 shows a set of images under an infrared (IR) microscope, comparing structures without and with XeF_2 etching for both SOI and single crystal silicon (SCS) test wafers. For SOI wafers, a clear cavity can be seen, while for SCS test wafers, the area that is etched appears black due to the rough etch front of XeF_2 isotropic etching. The trench color in an IR image can serve as an indicator of whether silicon inside the cavities of SOI wafers has been completely removed. As shown in Fig. 4(c), insufficient etching will result in the similar dark color due to the roughness on the surface of the remaining silicon.

After the releasing of the sacrificial silicon to create large gaps between structures in the device layer, oxide pillars are formed where the short slots have been etched in large trenches. While optional for smaller trenches (<30μm), these oxide pillars help with preventing the rupture and buckling of the thin oxide film for cavities with larger areas. Fig. 5 shows

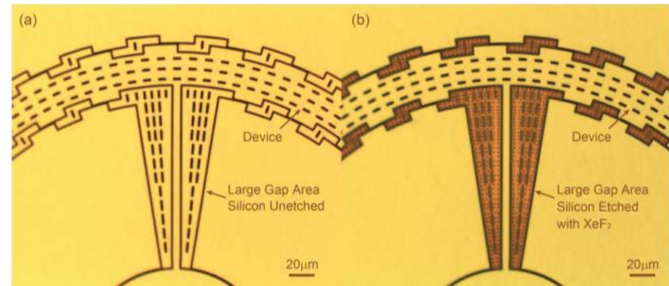

Fig. 3. Optical images of structures with oxide film on top and (a) without XeF_2 etching (without pin-holes); (b) with XeF_2 etching to remove the silicon in the large gap area.

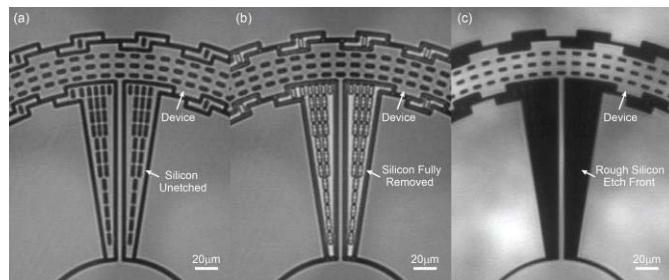

Fig. 4. IR images of a device (a) without XeF_2 etching; (b) 20μm SOI wafer with silicon fully etched with XeF_2; (c) A single crystal silicon test wafer with XeF_2 etching. Rough silicon etch front appears as dark under IR.

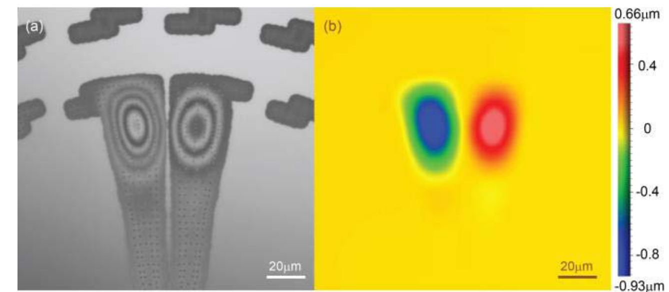

Fig. 5. (a) Fringe patterns show the topology of thin oxide film over the larger gap area without supporting oxide pillars; (b) Topology measurements indicating buckling of the oxide film without oxide pillars.

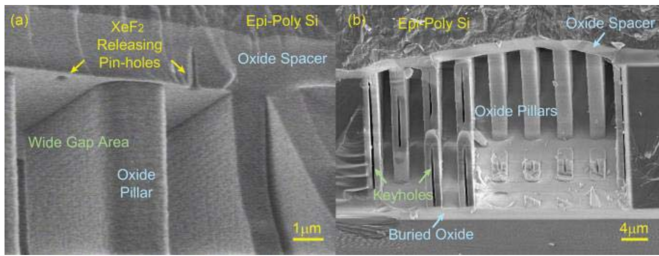

Fig. 6. Cross-sectional SEM images showing (a) fully sealed XeF_2 releasing pinholes; (b) oxide pillars in a 40μm wide trench encapsulated with polysilicon cap.

the topology measurement of the oxide film without the support of oxide pillars using the Zygo Nexview 3D Optical Surface Microscope. Large deformation of the oxide film is observed for large gap area, while there is no significant topology for smaller released areas. In comparison, Fig. 3 shows no obvious topology for structures with oxide pillar supports, demonstrating the effectiveness of oxide posts in improving the integrity of oxide film atop large gaps and in eliminating any buckling.

D. Sealing Pinholes With LPCVD Oxide Deposition

As shown in Fig. 1(e), the pinholes for XeF_2 etching are sealed by depositing 0.8μm of LPCVD TEOS oxide immediately after XeF_2 etching of sacrificial silicon. This results in a 2μm thick oxide spacer between the device layer and the encapsulation layer. SEM image (Fig. 6(a)) shows the completely sealed pinholes preventing any polysilicon depositing into the cavity. The sacrificial oxide inside the cavity, including the BOX oxide layer, the LPCVD oxide spacer and the oxide pillars, will be completely removed with vapor phase HF etching to release the movable structures of the MEMS devices in later steps.

E. Epitaxial Polysilicon Deposition

Using the Applied Material Centura Epitaxial Reactor with hydrogen as a carrier gas, epitaxial polysilicon encapsulation layer of 5μm is deposited as the first cap, as shown in Fig. 1(f). In order to deposit polycrystalline silicon on top of the oxide surface, a thin seed layer is first deposited with silane (SiH_4) as the precursor gas at 800°C and near atmospheric pressure. Then, dichlorosilane (DCS, SiH_2Cl_2) is used as a precursor and silicon is deposited at 1080°C and 30 torr to thicken the silicon layer to 5μm. Dopant gas, phosphine (PH_3) for N-type wafers or diborane (B_2H_6) for P-type wafers, flows at the same time to achieve heavily doped silicon layers for conducting electrical signals. As a result, the epitaxial polysilicon layer has a resistivity of around 3.5mΩ-cm for N-type and 1.5mΩ-cm for P-type wafers. SEM images (Fig. 6) show the cross-section of encapsulated wide gap areas with oxide pillars.

F. Creating Top Electrodes With Silicon Nitride

From this point, the rest of the process follows the same steps as the work described in [14]. As illustrated in Fig. 1(g), top electrode isolations are created with nitride plugs, which serve as an etch stop for the subsequent vapor HF etching and electrical isolation etching. These plugs allow for isolation of the cavity from the outside while maintaining electrical insulation of the defined top electrode area with the rest of the encapsulation cap. To create the nitride T-shaped plugs in the first cap layer, 2μm trenches are etched until the oxide spacer and are subsequently filled with $\sim 2.2\mu$m LPCVD low-stress silicon nitride. The silicon nitride film on top is then etched away to create the T-plugs.

To create electrical contacts to the device layer, 6μm wide vias are etched though the first cap with DRIE and 2μm thick oxide spacer is etched with an AMT 8100 Hexode plasma etcher. Around 9μm of epitaxial silicon is subsequently deposited to fill the electrical vias and to thicken the encapsulation layer. Chemical Mechanical Polishing (CMP) with Ultra-Sol S10 slurry is performed to remove uneven surface topology caused by nitride plugs and electrical vias.

G. Device Releasing

Small vent holes (0.8μm) are patterned and etched though the encapsulation layer using DRIE, as illustrated in Fig. 1(h). The sacrificial oxide surrounding the devices, including the BOX layer and the deposited LPCVD oxide, is released with an alcohol-based vapor phase HF etchant using the SPTS μetch vapor etch system (Fig. 1(i)). The oxide support pillars are completely removed during this step. Key holes inside the trenches (shown in Fig. 6(b)) allow vapor HF to access the buried oxide layer as soon as the top 2μm oxide film is etched. This results in similar etch rates for both top and bottom oxide layers, allowing silicon structures as wide as 18μm to be released. Etch holes are required if the released structures are to be larger. IR images of devices before and after vapor HF releasing are shown in Fig. 7. Images also show that the vapor HF etch front for both top and bottom are approximately 9μm away from the trenches. Compared to previous works that use wafer bonding to encapsulate the wide trenches [13], [14]—which suffered from vapor HF traveling though bonding interfaces and releasing undesired areas—the vapor HF etch front in this work is much better defined. This yields better defined anchors, which in turn contribute to the robustness of the process.

H. Device Sealing

The cavity is subsequently sealed with epitaxial polysilicon deposition and hydrogen annealing at 1130°C prior to the deposition (Fig. 1(j)). Differing from the epitaxial deposition recipe used in previous steps, no seed layer is deposited. Instead, a non-conformal selective recipe is used to prevent deposition on oxide and shorting of the device to the encapsulation layer or the wafer substrate. Around 3μm of silicon is deposited to seal all the vents using a recipe with a high HCl flow rate, which helps etching off any silicon nucleating on oxide and preventing deposition on the oxide surface. Another layer ($\sim 15\mu$m) of highly doped silicon is deposited after the sealing to thicken the cap for mechanical stability.

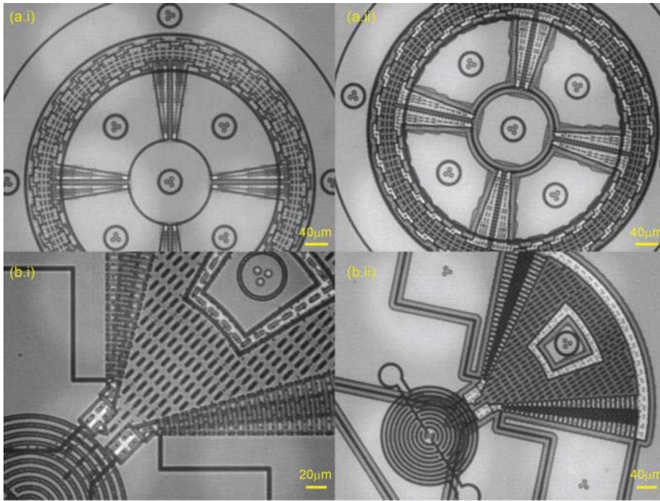

Fig. 7. IR images of various devices (a) wheel-shaped resonator and (b) wedge-shaped resonator (i) before, and (ii) after the vapor phase HF releasing of oxide. HF vapor etch fronts, both top and bottom, are clearly shown after the releasing.

As reported in previous *epi-seal* works, the high-temperature hydrogen environment during the annealing and epitaxial deposition steps removes native oxide from the device surface. Moreover, the high-temperature steps smoothen the device sidewalls through silicon migration, removing the surface roughness and scallops from DRIE. Finally, the sealing step ensures that the cavity is free of organics, humidity and oxygen.

The total cap thickness is approximately 30μm. CMP is performed again to smooth the top epitaxial polysilicon surface.

I. Electrical Connections and Hydrogen Diffusion

DRIE of isolation trenches in the encapsulation layer is performed to form isolation of electrical contact vias to the device layer and to define top electrodes (Fig. 1(k)). LPCVD low-stress silicon nitride is then deposited over the isolation trenches. The nitride deposition furnace provides a low-pressure (100mTorr), high-temperature (850°C) nitrogen environment, which diffuses out the remaining hydrogen in the cavity to create a low-pressure environment [14], [17]. More discussions regarding cavity pressure can be found in §III.B.

Electrical vias to the encapsulation cap are etched through the top silicon nitride layer. 1.5μm thick layer of Aluminum is then sputtered and patterned, forming electrical traces and wire-bond pads on the top surface. Final annealing step at 400°C in a nitrogen environment is performed for 3 hours.

At this point, all the devices are wafer-level encapsulated in an ultra-clean high vacuum environment and can be diced into individual dies for testing. In this work, the wafer was diced into 2mm × 2mm dies, which can be wire-bonded and tested in an ambient environment as shown in Fig. 8.

III. Results and Discussion

Using the described process, fully functional silicon MEMS devices with both wide and narrow trenches were fabricated.

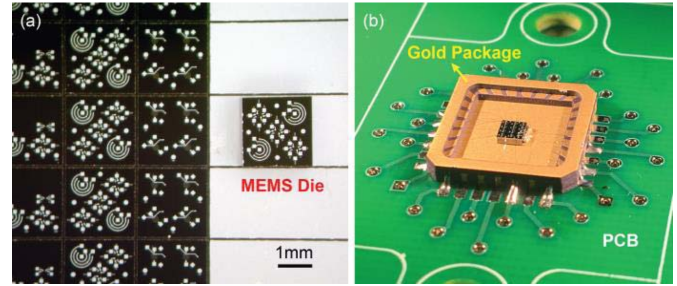

Fig. 8. (a) Diced devices; (b) Device wirebonded on a gold package and mounted onto a PCB.

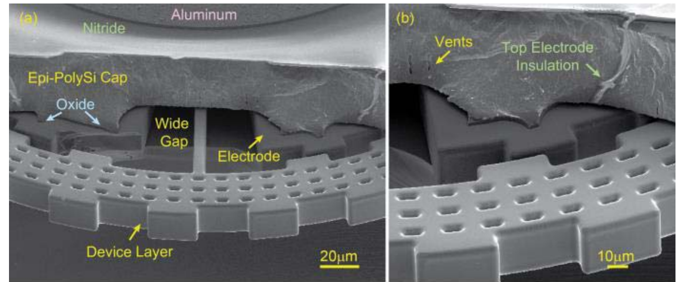

Fig. 9. Cross-sectional SEM images of (a) A fully encapsulated wheel-shaped resonator with wide lateral trenches for large deflection. (b) A zoomed-in view showing the sealed vent holes and top electrode isolation defined in the encapsulation layer.

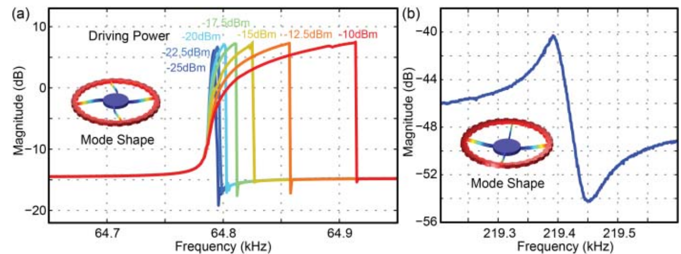

Fig. 10. (a) Open-loop frequency response of the large deflection wheel-shaped resonator's in-plane torsional mode; (b) Open-loop frequency response of the out-of-plane mode driven with top electrode and sensed with in-plane electrodes. Bias voltage for both measurements is 25V.

As an example, cross-sectional SEM images of a torsional wheel-shaped resonator is shown in Fig. 9. Gear-shaped electrodes are used to capacitively drive and sense the rotation of the structure. Both large and narrow lateral gaps are clearly shown in the SEM images, as well as top electrode insulations defined in the cap layer.

A. Frequency Response

Frequency response of the torsional resonator is shown in Fig. 10. The device is driven and sensed with the HP8753ES network analyzer. Open-loop responses of the in-plane torsional mode (at around 64.8kHz) driven with various powers are shown in Fig. 10(a). Large lateral gaps allow the resonator to be driven into extreme nonlinear region without contact or breakdown. Top electrodes enable driving and sensing of the out-of-plane modes (Fig. 10(b)).

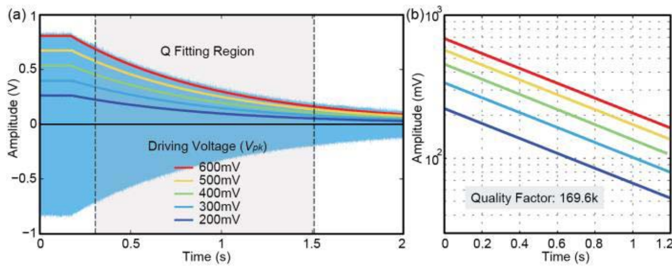

Fig. 11. (a) Ring-down measurements of the wheel-shaped resonator's in-plane torsional mode with different driving voltages. Amplitude curves extracted with FFT methods are plotted. Raw ring-down signal with 600mV driving voltage is shown in light blue. (b) Amplitude vs time for the Q fitting region. Quality factor is extracted to be 169.6k.

Ringdown measurement is conducted to measure the quality factor (Q) of the in-plane torsional mode. The resonator is first driven into resonance and phase-locked with the Zurich Digital Lock-in Amplifier. After switching off the AC excitation voltage, the output signal is recorded with the PicoScope digital oscilloscope (Fig. 11(a)). Using the FFT method detailed in [18], the amplitude information of the resonant frequency is tracked over time for different initial AC driving voltages. The extracted quality factor value for the torsional mode is around 169.6k (Fig. 11(b)).

To demonstrate the high yield of this process, 10 devices from different sections of the wafer are tested. 100% of the devices show expected frequency response, indicating the robustness of this work.

B. Cavity Pressure

As briefly mentioned in §II.I, previous research has shown that the cavity pressure for the epitaxially encapsulated devices is <0.1Pa [14] with the same diffusion steps as used in this work. To demonstrate the consistency between this process and the previous works, the cavity pressure is evaluated using quality factor (Q) as an indicator. The same wheel-shaped resonator is used for this measurement. The 2mm $\times$ 2mm die is attached and wire-bonded to a gold package. A 15μm $\times$ 15μm hole was drilled through the encapsulation cap using a focused ion beam (FIB) to vent the cavity. The vented device was mounted to a printed circuit board (PCB) and was then placed into a pressure chamber. The quality factor of the device as a function of pressure was measured using the ringdown method, as illustrated in Fig. 12. As shown, energy loss of the device is dominated by air damping at higher pressure. As the pressure decreases, energy is mainly lost through other mechanisms, such as thermoelastic dissipation (TED) or anchor loss. After a certain pressure level, the quality factor stops increasing with pressure drops. Based on the measurement, the cavity pressure is estimated to be <0.5Pa, which is consistent with the previous reported *epi-seal* processes [14], [17].

C. Stability and Fatigue

Long-term stability is a key feature for resonating MEMS devices. Previous studies have shown exceptional frequency stability of devices fabricated in *epi-seal* process [19], [20].

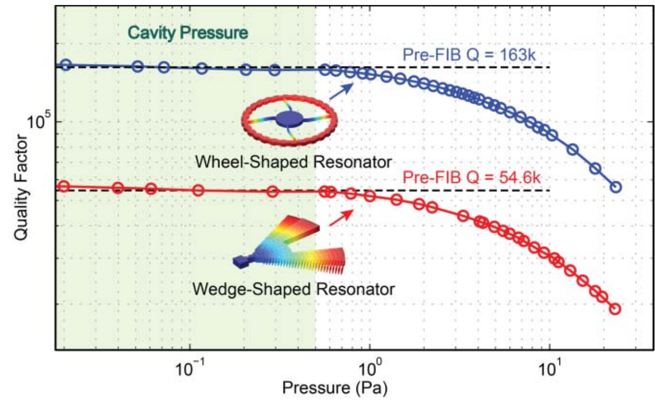

Fig. 12. Pressure vs. quality factor for both wheel-shaped resonator and wedge-shaped resonator. Dashed lines indicate measured Q values before venting the cavity with a focused ion beam.

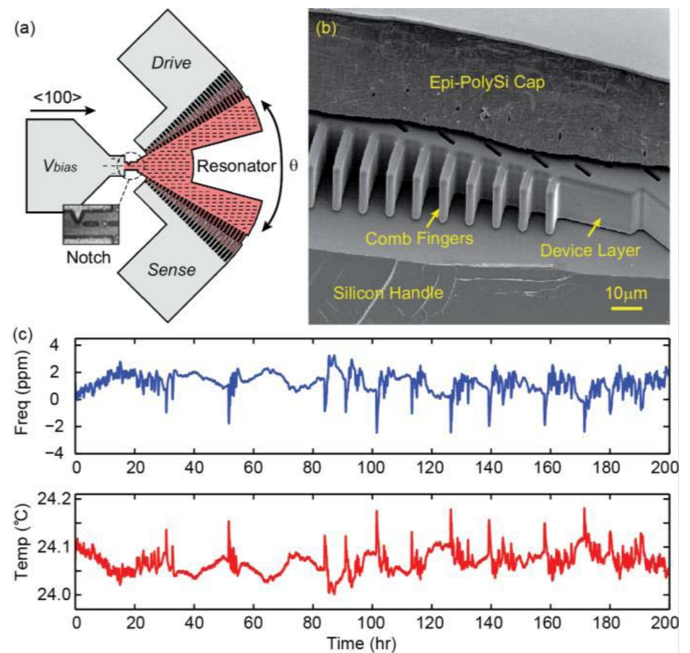

Fig. 13. (a) Design of the wedge-shaped resonator used as a fatigue test structure. The inset shows an IR image of the notch for stress concentration; (b) SEM image of the encapsulated wedge-shaped resonator with comb fingers (c) Frequency change and measured temperature over a testing period of 200hrs under maximum stress of 2.7GPa at the notch.

On the other hand, wide gaps enable the fabrication of devices with large lateral displacements, which cause large stress and in turn induce fatigue in silicon devices. Fatigue decreases the stiffness and consequently frequency of resonant systems [8]. Hence, for this fabrication process, it is important to demonstrate the frequency stability of devices under large stress.

Hong, *et al.*, [8] has previously shown the lack for fatigue for *epi-sealed* single crystal silicon devices fabricated with the wafer bonding-based process reported in [13]. Similar fatigue experiments are conducted with the devices fabricated from this work. As shown in Fig. 13, the fatigue test resonators consist of a wedge-shaped proof mass anchored though a cantilever aligned to the <100> orientation. Comb fingers used for capacitive driving and sensing are placed on both

TABLE I
WAFER BOW AT DIFFERENT STEPS

Step	Wafer State	Wafer Bowing (μm)
Fig. 1b	After Device Layer Pattern Etching	5.9
Fig. 1f	After First Cap Deposition	3.0
Fig. 1g	After Nitride Etching	10.9
Fig. 1h	After CMP Before Vents Etching	8.2
Fig. 1j	After Releasing, Sealing and CMP	-12.5

Positive wafer bowing indicates downwards bowing, while negative number indicates upwards bowing.

sides of the proof mass. A V-shaped notch in the middle of the cantilever concentrates the stress. The lock-in amplifier and a transimpedance amplifier (TIA) are used to drive and sense the resonator with a phase-locked loop (Fig. 13(b)) at the resonance frequency of 59.3kHz. A driving AC voltage of 1Vpk and a 10V bias voltage are used to resonate the device, with a stress level of ∼2.7GPa at the notch. The stress evaluation method is detailed in [8]. The device is operated in a convection oven with a controlled temperature at 25°C.

As shown in Fig. 13(c), over the test period of 200 hours—over 4.2e10 cycles—the frequency shift maintains within ±3ppm, which is within the expected error caused by the fluctuation of oven temperature. No fatigue behavior is observed, and the measured frequency stability is consistent with previously reported results of *epi-sealed* devices [19], [20].

D. Stress Caused Wafer Bowing During Fabrication Process

During the fabrication process, deposition and etching of stressed materials can cause the shape of the wafer to be concave or convex. Excessive wafer bow causes not only issues with wafer handling in various process tools, but also a decrease in alignment accuracy during photolithography. Throughout the fabrication, various thin films (oxide, nitride and highly-doped polysilicon) are deposited. Sacrificial materials (doped single crystal silicon, oxide) are also etched away. Moreover, the wafers go through multiple high-temperature annealing and CMP steps, making it important to demonstrate the absence of wafer bow issues throughout the process.

The wafer bow was measured at various steps as listed in Table 1. As shown, wafer bow is minimal throughout the entire process. This demonstrates that XeF_2 etching of large area of sacrificial silicon does not affect the overall strain in the wafer, contributing to the robustness of the process.

IV. Future Process Improvement

A. Achieving Etch Hole-Free Devices With Large Gaps

As mentioned in §II.G, etch holes are required to fully release large silicon structures. However, etch holes cause thermoelastic dissipation (TED), which limits the f-Q product of bulk acoustic-mode resonators. An etch hole-free process as a variation of *epi-seal* process has been previously reported [21]. This process begins with a SOI wafer with a thin (∼3μm) device layer; the buried oxide (BOX) under the large structure is firstly released with vapor HF. Subsequently, a thick epitaxial single crystal layer is deposited to seal the vHF vents and thicken the device layer. From this point, the fabrication follows the standard *epi-seal* process and allows only narrows trenches. It is worth noting that the process proposed in this work is compatible with the etch hole-free process reported in [21]. Combining the two processes can result in a unified *epi-seal* process that allows for large lateral trenches, etch hole-free structures and top electrodes, all without the need of wafer bonding.

Pre-fabricated cavity SOI [22] can also be used to replace the steps reported in [21]. In this case, both etch hole-free and large lateral gaps can be achieved at the same time by following the exact processes described in this work.

B. Limitations on Gap Size

As mentioned in previous sections, the fabrication technique reported in this work allows the encapsulation of devices with both wide and narrow trenches. However, given that the wide trenches are fabricated by etching away free-standing sacrificial silicon structures that are surrounded by oxide-filled narrow trenches, the narrowest free-standing silicon allowed and the widest trenches that can be filled with LPCVD oxide determine the achievable gap size. For the case in which the narrowest free standing structure is 2μm wide and the narrowest trench width that can be etched with DRIE is 0.5μm: if LPCVD oxide was deposited just enough to refill 1.5μm wide trenches, then the trench widths between 1.5μm and 3μm cannot be directly achieved. One possible solution is to simply deposit more sacrificial oxide to fill up to 3μm trenches. In such case, there is no restriction on gap size.

Even with the gap size limitations, however, the available trench widths suit the need for most purposes, including comb-drive structures, wide trenches for large lateral displacements, and narrow trenches for capacitive sensing.

V. Conclusion

This work demonstrates a robust wafer-level encapsulation process for the fabrication of single crystal silicon MEMS devices with large lateral gaps. Comb-drive structures and devices with large lateral displacements—devices previously precluded in standard *epi-seal* processes due to gap size limitations—are fabricated. Vapor phase XeF_2 isotropic etching of silicon is used to encapsulate wide gaps without the need of wafer bonding. This work demonstrates the robustness of the proposed method, and experiments reveal that fabricated devices preserve key benefits of the standard *epi-seal* process. In addition to the examples used in this paper, a wide range of devices, e.g. MEMS resonators [20], [23], [24], inertial sensors [25]–[28] and pressure sensors [29], [30] etc., can be co-fabricated and encapsulated with the proposed modified *epi-seal* process, making it a suitable process for fabricating MEMS combo sensors.

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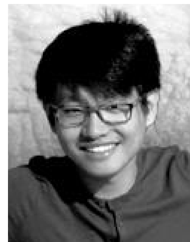

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